

DIALOG(R)File 347:JAPIO

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INSULATED GATE TYPE FIELD EFFECT SEMICONDUCTOR DEVICE

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JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)

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ABSTRACT

PURPOSE: To obtain characteristics similar to a single crystal semiconductor even in a thin film structure of a field effect semiconductor device by forming a channel forming region under a gate at a semi-amorphous semiconductor having fine crystallinity formed on a substrate.

CONSTITUTION: A pair of impurity regions 29, 30 are formed at both sides of a channel forming region on a semi-amorphous semiconductor 20 having fine crystallinity on a substrate 1. Gate electrodes 35 are formed on the channel forming region and an insulator 33. A field insulator 31 is formed on a pair of impurity regions 29, 30 forming a source and a drain.

DIALOG(R)File 352:DERWENT WPI
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Insulating gate type field effect transistor - has channel formed under
gate on fine crystal semi-amorphous semiconductor NoAbstract

Patent Assignee: HANDOTAI ENERGY KENKYUSHO KK (SEME)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
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Priority Applications (No Type Date): JP 81125003 A 19810810

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
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Title Terms: INSULATE; GATE; TYPE; FIELD; EFFECT; TRANSISTOR; CHANNEL;
FORMING; GATE; FINE; CRYSTAL; SEMI; AMORPHOUS; SEMICONDUCTOR;
NOABSTRACT

Derwent Class: U12

International Patent Class (Additional): H01L-029/78

File Segment: EPI